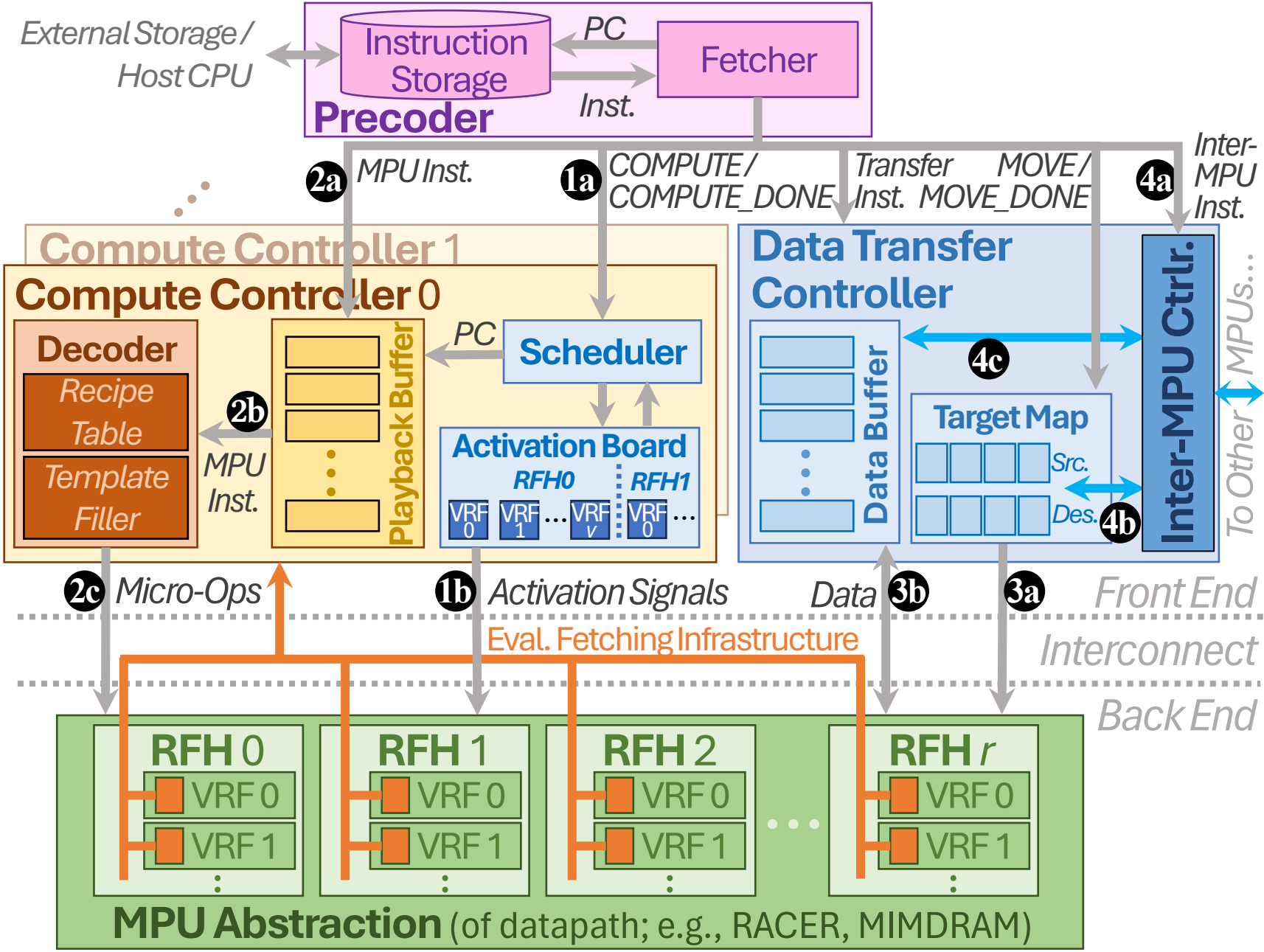
External Storage / Host CPU
Instruction Storage
PC
Fetcher
Inst.
Precoder
2a
MPU Inst.
1a
COMPUTE / COMPUTE_DONE
Transfer Inst.
MOVE / MOVE_DONE
4a
Inter-MPU Inst.
Compute Controller 1
Compute Controller 0
Decoder
Recipe Table
Template Filler
2b
MPU Inst.
Playback Buffer
PC
Scheduler
Activation Board
RFH0
RFH1
VRF 0
VRF 1
VRF v
VRF 0
Data Transfer Controller
Data Buffer
4c
Target Map
Src.
Des.
4b
Inter-MPU Ctrlr.
To Other MPUs...
2c
Micro-Ops
1b
Activation Signals
Data
3b
3a
Front End
Eval. Fetching Infrastructure
Interconnect
Back End
RFH 0
VRF 0
VRF 1
RFH 1
VRF 0
VRF 1
RFH 2
VRF 0
VRF 1
RFH r
VRF 0
VRF 1
MPU Abstraction (of datapath; e.g., RACER, MIMDRAM)