YIQIU SUN

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SUMMARY

- Computer Architecture Ph.D. student focused on bridging the gap between Processing-in-Memory (PIM) hardware and system development through data-parallel programming models and compilers
- Self-motivated individual with extensive full-stack experience across compilers, operating systems, architecture, and memory systems, demonstrated through diverse research projects and two industry internships
- Founding student of a new research group with end-to-end problem-solving skills, demonstrated by leading the full lifecycle of one of the group's first projects

EDUCATION

University of Illinois Urbana-Champaign — **Champaign, IL**
Ph.D in Computer Science, advisor: Saugata Ghose, GPA: 4.0 — *Expected Dec 2026*

University of Michigan — **Ann Arbor, MI**
B.S.E in Computer Engineering, Summa Cum Laude, GPA: 3.9 — *Sep 2019 - May 2021*

Shanghai Jiao Tong University, UM-SJTU Joint Institute — **Shanghai, China**
Bachelor of Engineering in Electrical and Computer Engineering — *Sep 2017 - Aug 2021*

WORK EXPERIENCE

GPU Architecture PhD Intern — **Santa Clara, CA**
NVIDIA Corporation. Manager: Sangeetha Veerappan — *May 2025 - Aug 2025*

- Designed a traffic profiler in NVIDIA's full-chip simulator to evaluate interconnect scalability and developed a visualization framework that enabled software-hardware co-design in advanced packaging, supporting collaboration across architecture, software, and layout teams
- Rapidly onboarded to a large internal codebase and leveraged NVIDIA's internal infrastructure and AI tools to integrate solutions into the company's development workflow

Storage Systems Research Intern — **San Jose, CA**
Samsung Semiconductor, Inc. Manager: Shuyi Pei — *May 2023 - Aug 2023*

- Led an independent research project to redesign caching in CXL-SSDs, Samsung's next-generation memory-semantic storage device. Proposed and prototyped a novel scheme that significantly reduced embedding table lookup latency in recommender systems, resulting in a patent filing

RESEARCH EXPERIENCE

ARCANA Research Group, PI: Prof. Saugata Ghose — **Urbana, IL**

Programming Models for Processing-Using-Memory — *Jan 2022 - Aug 2025*

- Collaborated with Samsung researchers to establish a high-level parallel programming model to harness the massive performance and energy benefits of PUM architectures at scale
- Extended MapReduce to automate data partitioning and runtime tuning for PUM workloads, reducing communication and improving parallelism through algorithmic innovations

Support End-to-End Execution for Processing-Using-Memory — *Sep 2024 - Jul 2025*

- Co-led a lab-wide effort to build the first open-source cross-stack PUM system simulator (MASTODON)
- Independently built an advanced assembler to simplify complex control instructions including loops, branches, and subroutine calls; designed a frontend controller architecture to unify execution across diverse PUM datapaths

Computer Engineering Lab, PI: Prof. Trevor Mudge **Ann Arbor, MI**

Application of Deep Learning Algorithms on Transmuter *Jan 2020 - Aug 2020*

- Simulated RNN on gem5 for the Transmuter: a reconfigurable data flow accelerator, optimized hardware performance (GFLOPs) and total runtime through parallelism

PUBLICATIONS, PREPRINTS & POSTERS

Y. Sun*, T. Patabandi, S. Ghose. *MaRIMBA: A Framework to Manage Processing-Using-Memory Architectures at Scale.* Submitted to ASPLOS'26, preprint available upon request.
M.S.Q. Truong, Y. Sun* et al. *Supporting End-to-End Application Execution With a Generalized Interface for Processing-Using-Memory.* Submitted to HPCA'26, preprint available upon request.
Y. Sun*. *MapReduce Framework for Processing-Using-Memory.* Poster, PACT'24 SRC.
ARCANA Research Group*, Sandia National Laboratories. *Tutorial on Simulation for Processing-Using-Memory Systems.* ISCA'24 Workshop.
T. J. Baker, Y. Sun*, J. P. Hayes. *Benefits of Stochastic Computing in Hearing Aid Filterbank Design.* BioCAS'21, pp. 1-5, doi: 10.1109/BioCAS49922.2021.9645021.

CATEGORIZED PROJECT EXPERIENCE

Compiler / Programming Models

- ***Codelet-based Compiler Optimization*** (Prof. David Kuck, Intel+UIUC collab): Evaluated hardware performance across C compiler toolchains; generalized compiler optimization rules for broader search space
- ***Lowering Python APIs to AI Engines*** (Prof. Vikram Adve, AMD+UIUC collab): Built performance models for AMD Versal AI engines; explored design space beyond polyhedral scheduling
- ***Application of ML Kernels on PUM*** (Prof. Saugata Ghose): Designed frameworks to expose parallelism for ML workloads (e.g., LayerNorm, PCA, recommender) on memory-centric architectures

Operating Systems / System Software

- ***Hardware-Aware Paging*** (Prof. Tianyin Xu): Visualized DRAM bank usage to improve page allocation efficiency and memory level parallelism in multi-application environments
- ***OS/Memory Policy for 3D-Stacked DRAM/PCM*** (Prof. Jian Huang): Modeled thermal-induced memory errors from logic layer; proposed OS-level scheduling policies to mitigate or exploit heat effects

Architecture & Accelerator Design

- ***Depth Fusion Accelerator on Hybrid Memory Cube*** (Prof. Saugata Ghose): Designed and optimized a custom depth fusion hardware accelerator integrated into 3D-stacked memory logic layers
- ***N-Way Superscalar R10K Processor*** (Prof. Mark Brehob): Built an OoO processor RTL with complex branch predictor, prefetcher and non-blocking cache; developed a GUI debugger for CPI analysis

SKILLS & ABILITIES

Languages/Applications: C/C++, SystemC, SystemVerilog, Python, CUDA, Perl, Go, MATLAB, OCaml, Hadoop, Halide, Bash script
Architectural Simulators: (PIM+)Ramulator, Gem5, MQSim, zsim, DRAMPower, SST Simulator
Courses: Emerging Memory/Storage System, Distributed Systems, System-On-Chip Design, Architecture for Mobile & Edge Computing, Language & Compilers for Edge Computing, Prgm Languages & Compilers

SERVICE & OUTREACH

Co-organizer of Women-In-Arch at UIUC *Jan 2024 - present*
Graduate Student Ambassador at UIUC CS *Spring'22, Spring'23*
Teaching Assistant, *Computer System Organization (CS 433)* by Prof. S. Ghose *Spring'24, Fall'25*
Artifact Evaluation for MICRO'23, ASPLOS'25
Undergraduate/Graduate Mentor, UIUC *(mentored 5 students)* *Jan. 2022 - present*