YIQIU SUN

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SUMMARY

- Computer Architecture Ph.D. student focusing on bridging the gap between processing-in-memory hardwares and system development through data-parallel programming models
- Self-motivated individual with extensive full-stack experience in Interconnect Network, Memory and Storage Systems and Hardware-Software Co-design evidenced by multiple research projects and one industrial internship
- Founding student of a new research group with end-to-end problem-solving skills demonstrated by leading a whole life circle of one of the first projects in group

EDUCATION

University of Illinois Urbana-Champaign — **Champaign, IL**
Ph.D in Computer Science — *Expected May 2027*
· Advisor: Saugata Ghose

University of Michigan — **Ann Arbor, MI**
B.S.E in Computer Engineering, Summa Cum Laude — *Sep. 2019 - May 2021*
· Advisor: Mark Brehob

Shanghai Jiao Tong University, UM-SJTU Joint Institute — **Shanghai, China**
Bachelor of Engineering in Electrical and Computer Engineering — *Sep. 2017 - Aug. 2021*
· Advisor: Weikang Qian

RESEARCH EXPERIENCE

Programming Models for Processing-In-Memory (Paper Under Submission) — **Urbana, IL**
Advisor: Prof. Saugata Ghose — *Jan. 2022 - present*
· Build a cycle-accurate simulator for a general digital Processing-Using-Memory (PUM) architecture
· Explore the implementation of data-parallel programming models framework on PUM and identify new design points
· Model and optimize a low-latency, highly-scalable, and well-balanced interconnect network for PUM architecture
· **Preliminary work presented in CSL Student Conference'24 and Student Research Competition PACT'24**
· **Simulator tutorial presented in ISCA'24 Workshop: Simulation for Processing Using Memory Systems**

Stochastic Circuits Implementation of Filter Banks Used in Hearing Aids — **Ann Arbor, MI**
Advisor: Prof. John P. Hayes — *May 2020 - Aug. 2021*
· Implemented a stochastic circuit version of filter bank used in hearing aids and used Synopsys to synthesis the circuits
· Minimized matching error while maintaining the advantage of stochastic circuits in area and energy cost

Application of Deep Learning Algorithms on Transmuter — **Ann Arbor, MI**
Advisor: Prof. Trevor Mudge — *Jan. 2020 - Aug. 2020*
· Simulated RNN on gem5 for the Transmuter, a reconfigurable data-flow accelerator
· Optimized hardware performance (GFLOPs) by 20% and total runtime by 50% through parallelism

WORK EXPERIENCE

Storage Systems Architect Intern — **San Jose, CA**
Samsung Semiconductor, Inc. — *May 2023 - Aug. 2023*
· Worked on an independent research project related to the caching scheme in CXL-SSD (patent pending)
· Selected as Samsung Global Star for a one-week business trip to South Korea

SELECTED PROJECT EXPERIENCE

Edge Computing on ECRAM-based Architecture **Urbana, IL**
Advisor: Prof. Saugata Ghose *Sept. 2023 - present*
· Help co-design a continual-learning-based Simultaneous Localization and Mapping algorithm with a cost-effective analog in-memory computing architecture
· Aim to achieve an end-to-end physical implementation based on a fabricated ECRAM chip

Codelet-based Compiler Optimization Space Exploration **Urbana, IL**
With Intel Corporation, Advisor: Prof. David Kuck *Nov. 2021 - Dec. 2023*
· Generalized hardware saturation rules based on different codelet types to enlarge optimization search space of a compiler
· Helped develop a tool to automate the process from codelet generation to experimental data analysis

Analyzing the Impact of Processing-in-Memory Devices on Scene Reconstruction **Urbana, IL**
Advisor: Prof. Saugata Ghose *Feb. 2022 - April 2022*
· Evaluated two different depth fusion algorithms executing on a conventional CPU+memory system and a Hybrid Memory Cube with standard CPU cores
· Designed a custom hardware accelerator for depth fusion that can be built into the logic layer of a 3D-stacked memory

Algorithms and Optimizations for Lowering Python Package APIs to AI Engine Array **Urbana, IL**
Advisor: Prof. Vikram Adve *Feb. 2022 - April 2022*
· Established specialized performance modeling for AI engines
· Scheduled high-level NumPy logic onto AI engines which explores a more exhaustive design space than polyhedral model

N-Way Superscalar R10K Out-of-Order Processor **Ann Arbor, MI**
Advisor: Prof. Mark Brehob *March 2020 - April 2020*
· Built an N-way Superscalar R10K Processor with a complicated branch predictor, non-blocking caches and prefetching
· Developed a GUI debugger to visualize CPU workflow and speed up debugging process
· Performed a thorough analysis of CPU performance (CPI) with regard to number of ways and component sizes

PUBLICATIONS & WORKSHOPS

T. J. Baker, **Y. Sun** and J. P. Hayes, "Benefits of Stochastic Computing in Hearing Aid Filterbank Design," 2021 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2021, pp. 1-5, doi: 10.1109/BioCAS49922.2021.9645021.

SKILLS & ABILITIES

- **Languages/Applications**: C, C++, System Verilog, Python, CUDA, Go, MATLAB, Ocaml, Hadoop
- **Board**: Arduino, FPGA (PYNQ), PSoC
- **Architectural Simulator**: (PIM+)Ramulator, Gem5, MQSim, zsim, DRAMPower, SST Simulator
- **Courses**: Emerging Memory/Storage System, Distributed Systems, System-On-Chip Design, Architecture for Mobile & Edge Computing, Language & Compilers for Edge Computing, Programming Languages & Compilers

TUTORING & VOLUNTEERING EXPERIENCE

Co-organizer of Women In Arch at UIUC *Jan. 2024 - present*
Graduate Student Ambassador at UIUC CS *Jan. 2022 - present*
Teaching Assistant, *Computer System Organization (CS 433)* by Prof. Saugata Ghose *Jan. 2024 - May 2024*
Member of MICRO'23 Artifact Evaluation Committee *Aug. 2023 - Sep. 2023*
Undergraduate/Graduate Mentor, UIUC
· Nandini Rao, CS'27 (SRC Research Scholar) *Aug. 2024 - present*
· Vijay Shah, CS Master *April 2024 - present*
· Phyllis Wang, CS'24 (DaRin Butz Foundation Research Scholar), now at Princeton *March 2023 - May 2024*
· Tianyun Zhang, CS+Economics'23, now at CMU *Jan. 2022 - May 2023*